IN THE SPECIFICATION:

Replace the paragraph starting at page 7, line 17 as follows:

Referring to FIG. 2, the codec apparatus includes a codec 210, a channel selector 212 for generating a channel select signal, S_FS and a first mixer 214 and a second mixer 216. The channel selector 212 outputs the channel select signal S_FS and mixing control signals J and K, which are controlled by a clock signal CLKx, a frame sync signal FSx, an read address, and data input. One skilled in art would know that ~~that~~ there are various ways and type of circuits served to provide an address generator controlled by a clock signal from a clock domain, which can generate read address for reading out data from the data storage elements. The codec 210 has input/output terminals for receiving and supplying the A-law modulated digital signals B and D, respectively, and input/output terminals for receiving and supplying the Φ-law modulated digital signals A and C, respectively. The codec 210 selectively converts a specified channel signal from the modulated multi channel signals in response to the channel select signal, S_FS generated by the channel selector 212. The first mixer 214 includes two buffers operating complementarily to each other in response to the mixing control signal J, a first buffer 214a for storing the digital signal output E from the codec 210 and a second buffer 214b for storing the original digital signal B. Similarly, the second mixer 216 consists of two

buffers operating complementarily to each other in response to the mixing control signal K, a third buffer 216a for storing the digital signal output H from the codec 210 and a fourth buffer 216b for storing the original digital signal C. Each pair of the buffers in each mixer share the output terminal and operate complementarily to each other in such a manner that first buffer is enabled while the second buffer is disabled, and vice versa.